

We Claim:

1. A method for fabricating a double gate MOSFET, which comprises the steps of:

providing a substrate structure having a silicon substrate layer, a first insulation layer disposed on the silicon substrate layer, a first spacer layer disposed on the first insulation layer, and a semiconductor layer disposed on the first spacer layer;

patterning the semiconductor layer resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET;

depositing a second spacer layer on the semiconductor layer structure and the first spacer layer;

patterning the first and second spacer layers such that the semiconductor layer structure remains substantially completely embedded in the first and second spacer layers;

depositing a second insulation layer on a structure formed of the first and second spacer layers;

vertically etching two depressions disposed along one direction, the two depressions dimensioned such that the

semiconductor layer structure is situated completely between them, during the etching of the two depressions, the second insulation layer, the first and second spacer layers and, in each case on both sides, an edge section of the semiconductor layer structure being etched through completely in each case;

filling the depressions with an electrically conductive material;

forming a contact hole in the second insulation layer;

selectively removing the first and second spacer layers through the contact hole made in the second insulation layer;

applying third insulation layers on inner walls of a region of removed spacer layers and on surfaces of the semiconductor layer structure; and

introducing a further electrically conductive material into the region of the removed spacer layers.

2. The method according to claim 1, which comprises forming the substrate structure by applying the first insulation layer, the first spacer layer, and the semiconductor layer one after another.

3. The method according to claim 2, which comprises recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam.

4. The method according to claim 1, which comprises forming the substrate structure by the steps of:

providing the silicon substrate functioning as a first semiconductor substrate;

applying the first insulation layer on the first semiconductor substrate;

providing a second semiconductor substrate;

applying the first spacer layer on the second semiconductor substrate;

connecting the first and second semiconductor substrates to one another using a wafer bonding process between the insulation layer and the first spacer layer; and

reducing a thickness of the second semiconductor substrate resulting in the semiconductor layer.

5. The method according to claim 1, which comprises forming the first and second spacer layers from silicon nitride.
6. The method according to claim 1, which comprises planarizing the second insulation layer after being deposited.
7. The method according to claim 1, which comprises carrying out the step of selectively removing the first and second spacer layers through the contact hole made in the second insulation layer.
8. The method according to claim 1, which comprises forming the electrically conductive material from a material selected from the group consisting of doped polycrystalline silicon, metal and silicide.
9. The method according to claim 8, which comprises forming the doped polycrystalline silicon by chemical vapor phase deposition and a doping is performed during the deposition.
- b. 10. The method according to claim 1, which comprises using a selectively acting, wet-chemical etching step for removing the first and second spacer layers.
11. The method according to claim 1, which comprises applying the third insulation layers using a thermal oxidation process.

12. The method according to claim 11, which comprises producing a relatively thin oxide layer on the surface of the semiconductor layer structure and producing a relatively thick oxide layer on the inner walls of the region of the removed spacer layers.

13. The method according to claim 1, which comprises forming the further electrically conductive material from a material selected from the group consisting of doped polycrystalline silicon, metal and silicide.

14. The method according to claim 13, which comprises forming the doped polycrystalline silicon by chemical vapor phase deposition and a doping is performed during the chemical vapor phase deposition.

15. The method according to claim 1, which comprises applying an oxide layer as the first insulation layer.

16. The method according to claim 1, which comprises applying a silicon layer as the semiconductor layer.

17. The method according to claim 1, which comprises depositing an oxide layer as the second insulation layer.

18. The method according to claim 1, which comprises applying oxide layers as the third insulation layers.

19. The method according to claim 9, which comprises using arsenic atoms in the doping process.

20. The method according to claim 14, which comprises using phosphorous atoms in the doping process.

21. A double gate MOSFET, comprising:

a substrate;

a first insulation layer disposed on said substrate;

a semiconductor layer structure having horizontal surfaces and vertical surfaces;

a gate electrode disposed on said first insulation layer and said gate electrode completely surrounding said horizontal surfaces of said semiconductor layer structure, said semiconductor layer structure embedded in said gate electrode;

a source region disposed on said first insulation layer;

*not elected*

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a drain region disposed on said first insulation layer, said source region and said drain region disposed on opposite sides of said semiconductor layer structure and of said gate electrode, said source region and said drain region being contact-connected to said vertical surfaces of said semiconductor layer structure;

a second insulation layer disposed on said first insulation layer and said gate electrode, said second insulation layer having a contact hole formed therein for making contact with said gate electrode in a region of said gate electrode at a lateral distance from said semiconductor layer structure; and third insulation layers disposed on said gate electrode, said source region and said drain region.

22. The double gate MOSFET according to claim 21, wherein at least one of said gate electrode, said source region, and said drain region are formed from a material selected from the group consisting of doped polycrystalline silicon, metal and silicide.

23. The double gate MOSFET according to claim 21, wherein said substrate is a silicon substrate.

24. The double gate MOSFET according to claim 21, wherein  
said first insulation layer is an oxide layer.

25. The double gate MOSFET according to claim 21, wherein  
said second insulation layer is an oxide layer.